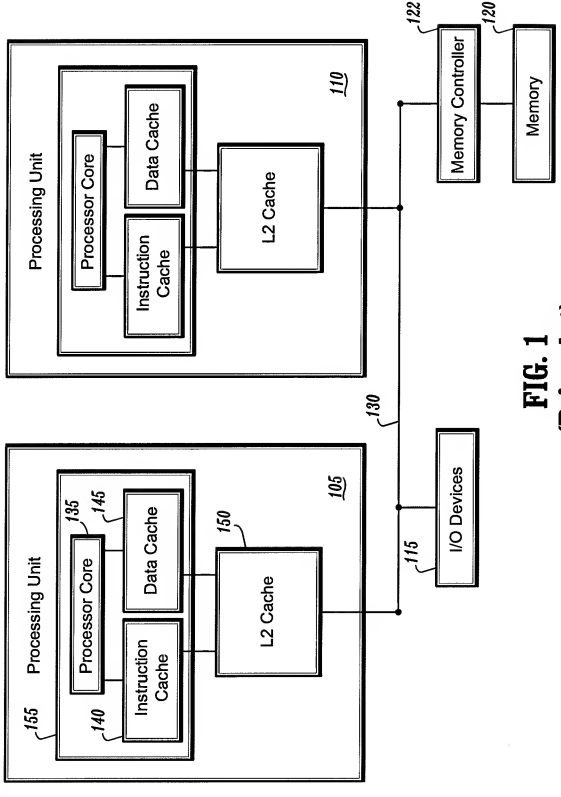

FIG. 1
(Prior Art)

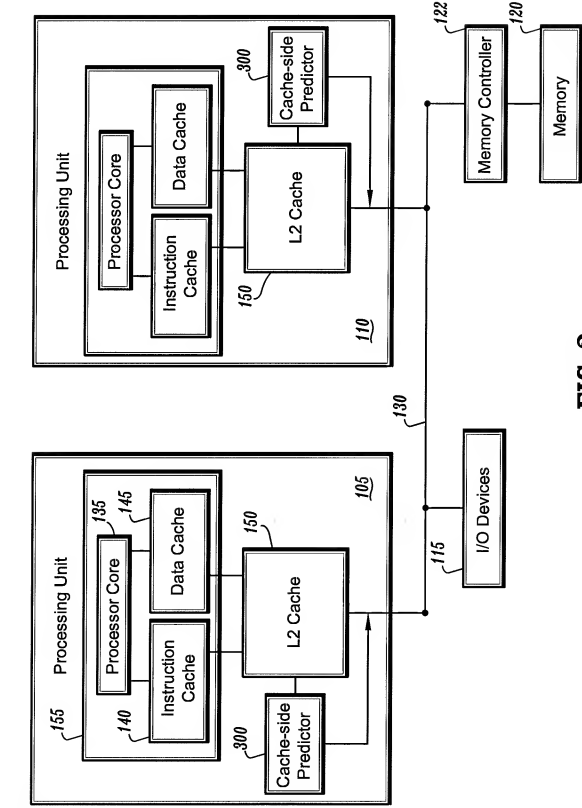
100
Processing Unit
155
Processor Core
135
Instruction Cache
140
Data Cache
145
L2 Cache
150
Cache-side Predictor
300
105
Processing Unit
Processor Core
Instruction Cache
Data Cache
L2 Cache
150
Cache-side Predictor
300
110
130
I/O Devices
115
Memory Controller
122
Memory
120

FIG. 2

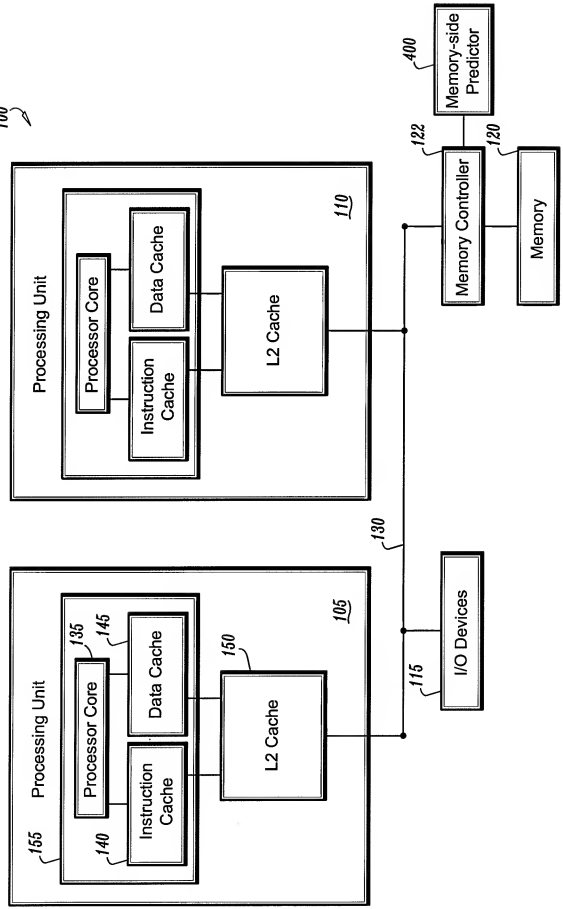
100
Processing Unit
Processor Core
Instruction Cache
Data Cache
L2 Cache
110
Processing Unit
155
135
145
140
150
105
130
115
I/O Devices
122
Memory Controller
120
Memory
400
Memory-side Predictor

FIG. 3

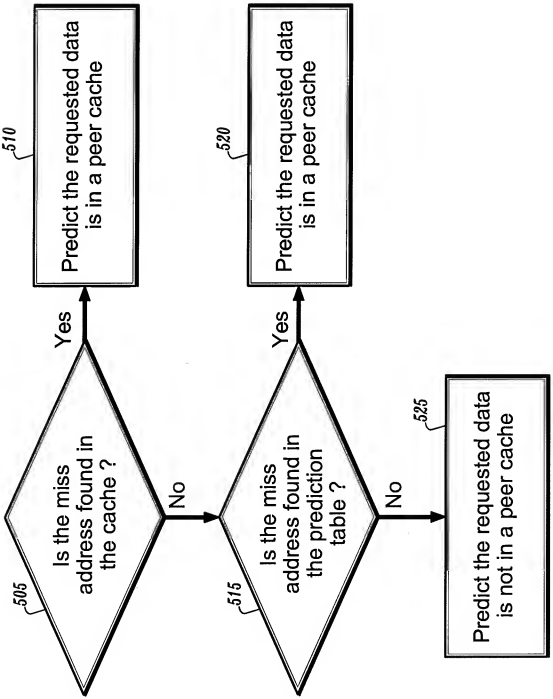
505
Is the miss address found in the cache ?
Yes
510
Predict the requested data is in a peer cache
No
515
Is the miss address found in the prediction table ?
Yes
520
Predict the requested data is in a peer cache
No
525
Predict the requested data is not in a peer cache

FIG. 4

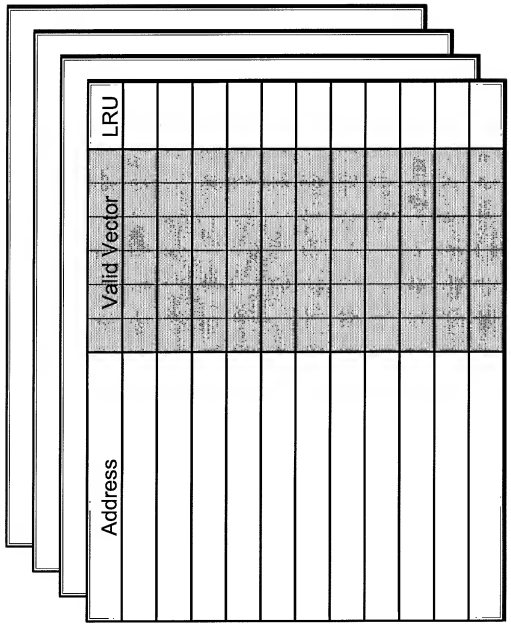

FIG. 5

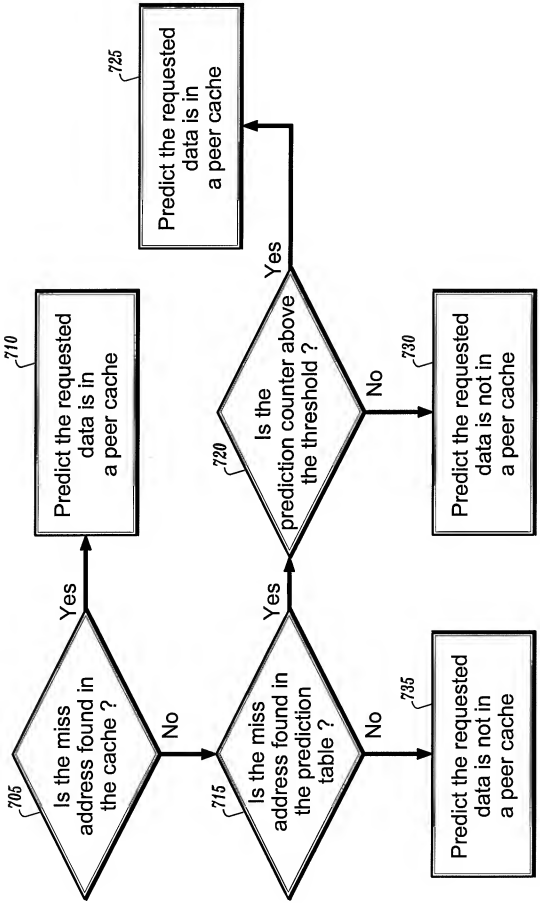
705
Is the miss address found in the cache ?
Yes
No
710
Predict the requested data is in a peer cache
715
Is the miss address found in the prediction table ?
Yes
No
720
Is the prediction counter above the threshold ?
Yes
No
725
Predict the requested data is in a peer cache
730
Predict the requested data is not in a peer cache
735
Predict the requested data is not in a peer cache

FIG. 6

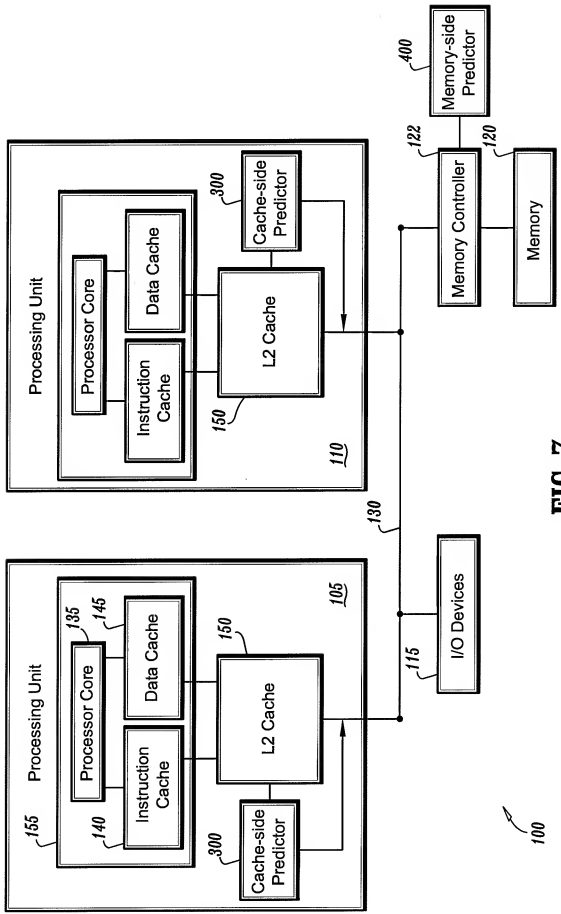
100
155
Processing Unit
140
Processor Core
135
145
Instruction Cache
Data Cache
150
L2 Cache
300
Cache-side Predictor
105
115
I/O Devices
130
Processing Unit
Processor Core
Instruction Cache
Data Cache
L2 Cache
150
300
Cache-side Predictor
110
122
Memory Controller
120
Memory
400
Memory-side Predictor

FIG. 7